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EXAMINER	
MAI, ANH D	
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SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/14/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/392,034	GONZALEZ ET AL.	
	Examiner	Art Unit	
	Anh D. Mai	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 December 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-22,24-27,31-40,42 and 43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3-22, 24-27, 31-40, 42 and 43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Status of the Claims

1. Amendment filed December 11, 2006 is acknowledged. Claims 1, 7, 11, 12, 14, 15, 18, 19-21, 24-26, 31-36, 38, 40, 42 and 43 have been amended. Claims 1, 3-22, 24-27, 31-40, 42 and 43 are pending.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 9, 10, 12 and 13 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

With respect to claims 9, 10, 12 and 13, there does not appear to be a written description of the claim limitation "removing the first dielectric layer using an etch recipe that etches the *first dielectric layer* faster than the *conformal layer and the spacers* by a ratio in a range about 1:1 to about 2:1; or 1.3:1 to about 1.7:1" in the application as filed.

PLEASE NOTE: the specification on page 14 discloses: "A first preferred selectivity of an etch recipe used in the inventive method is in the range of about 1:1 to 2:1, wherein **isolation**

film 36 (claimed as conformal layer) **is removed faster** as compared to **insulator island** (claimed as first dielectric layer). A more preferred selectivity is in the range of about 1.3:1 to about 1.7:1. A most preferred selectivity is about 1.5:1. Planarization also requires the etch recipe to remove **spacer 28** slightly faster than **insulator island 22**. Preferably, spacer 28 and insulator film 36 are made from the same material such that the etch will be substantially uniform as to the selectivity thereof with respect to spacer 28 and isolation film 36 over insulator island 22. (Emphasis added).

Applicant refers to page 17 for support. However, **Where is the etch ratio as claimed** ?

Applicant must provide support for or cancel the new matters.

This is a repeated rejection.

With respect to claim 21, there does not appear to be a written description of the claim limitation "**further comprising**, prior to filling each the isolation trench with the conformal third layer, forming a liner upon a sidewall of each the isolation trench" in the application as filed.

Claim 18 recites: "**rounding the top edges** of each the isolation trenches"

According the specification, **page 12**, thermal oxidizing the substrate forms the liner and rounding of the top edges *at the same time*. Therefore, by claiming **rounding the top edges**, the limitation of claim 18, implicitly includes the liner formed by thermal oxide.

Page 12, lines 14-17, is an alternative of forming liner by CVD, instead of thermal oxide.

Claim 21, however, adding "**further comprising**...forming a liner" means additional process **in addition to** liner already formed by thermal oxidation, "rounding the top edges".

Applicant must provide support for two process steps that rounding the top edges and a CVD liner (?) over the thermal liner.

As clearly claimed in claim 22, "the liner is a thermally grown oxide".

Claim 21 does not have support, thus, new matter.

This is a repeated rejection.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 9, 10, 12 and 13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Applicant refers to page 17 for support. However, this etching process does not have a specific etch ratio as claimed. The claimed etch ratios, however, are for removing the conformal layer.

Applicant appears to mix-and-match the etching of nitride material using the etch ratio of oxide material at a different process step, removing nitride layer.

As discussed above, the limitations of these claims are **contradicting what has been disclosed**, therefore, the claims are indefinite. See claim 26.

This is a repeated rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claim 38 is rejected under 35 U.S.C. 102(e) as being anticipated by Omid-Zohoor et al. (U.S. Patent No. 6,097,072) of record.

With respect to claim **38**, Omid-Zohoor '072 teaches a method for forming a microelectronic structure as claimed including:

providing a semiconductor substrate (120) having a top surface with an oxide layer (340) thereon; (Fig. 3B);

forming a first layer (344) upon the oxide layer (340); (Fig. 3C);

selectively removing the first layer (344) to expose the oxide layer (340) at a plurality of areas; (Fig. 3E);

forming a plurality of isolation trenches (360) through the oxide layer (340) at the plurality of areas, wherein an electrically insulative material (364) extends continuously between and within the plurality of isolation trench, each isolation trench (360):

having a spacer (356) composed of dielectric material upon the oxide layer (340) in contact with the first layer (344); (Fig. 3H);

extending from an opening thereto at top surface of the semiconductor substrate (120) and below the oxide layer (340) into and terminating within the semiconductor substrate adjacent to and below the spacer (356); (Fig. 3I);

having a second layer (364) filling the isolation trench (360) and extending above the oxide layer (340) in contact with the spacer (356), wherein the filling is performed by depositing the second layer (364), and the depositing is carried out to the extend of filling each isolation trench and extending over the spacer (356) and over the first layer (344); so as to define an upper surface contour of the second layer (364); (Fig. 3J); and

having a planar upper surface formed from the second layer (364) and the spacer (356) and being situated above the oxide layer (340); wherein the planar upper surface is formed by substantially simultaneously subjecting the entire upper surface contour of the conformal layer to a planarizing process; (Fig. 3M); and

wherein the microelectronic structure is defined at least in part by the plurality of spacers (356), the second layer (364), and the plurality of isolation trenches. (See Figs. 3A-M).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims **1**, 3-22, 24-26 and 31-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Omid-Zohoor '072 in view of Poon et al. (U.S. Patent No. 5,387,540) all of record.

With respect to claim **1**, Omid-Zohoor '072 teaches a method of forming a microelectronic structure substantially as claimed including:

forming an oxide layer (340) upon a semiconductor substrate (120);

forming a first dielectric layer (344) upon the oxide layer (340);

selectively removing the first dielectric layer (344) to exposed the oxide layer (340) at a plurality of areas;

forming a second dielectric layer (352) over the oxide layer (340) and the first dielectric layer (344), wherein forming the second dielectric layer (352) includes forming the second dielectric layer (352) over and in contact with the exposed oxide layer (340) at the plurality of areas;

selectively removing the second dielectric layer (352) to form a plurality of spacers (356) from the second dielectric layer (352), wherein each spacer (356) is situated upon the oxide layer 340), is in contact with the first dielectric layer (344), and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches (360) extending below the oxide layer (340) into the semiconductor substrate (120), wherein each the isolation trench (360) is adjacent to and below the pair of the spacers (356) and is situated at a corresponding area of the plurality of areas, and wherein each isolation trench (360) has a top edge;

filling each isolation trench (360) with a conformal layer (364), the conformal layer extending above the oxide layer (340) in contact with a corresponding pair of the spacers (356), wherein the filling is performed by depositing the conformal layer (364), and the depositing is carried out to the extent of filling each isolation trench (360) and extending over the spacers (356) and over the first dielectric layer (344) so as to define an upper surface contour of the conformal layer (364); and

substantially simultaneously subjecting the entire upper surface contour of the conformal layer to a planarizing process and planarizing the conformal layer (364) at least to the first dielectric layer (344) and each spacer (356) to form therefrom an upper surface for each isolation trench (376) that is co-planar to the other upper surfaces;

wherein the conformal layer (364) comprises a material that is electrically insulative extends continuously between and within the plurality of isolation trenches (360). (See Figs. 3A-M).

Thus, Omid-Zohoor '072 is shown to teach all the features of the claim with the exception of forming a liner upon the sidewall of each isolation trench.

However, Poon teaches that it is well known in the art to form a liner (28) upon the sidewall of each isolation trench (22) to remove damage caused by the trench-etch. (See Fig. 4).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to form the liner upon the sidewall of each isolation trench of Omid-Zohoor '072 as taught by Poon to remove the damage caused by the trench-etch.

With respect to claim 3, the liner (28) of Poon is thermally grown oxide of the semiconductor substrate.

With respect to claim 4, the liner (28) of Poon comprises deposition of a composition of matter (50). (See Fig. 11).

With respect to claim 5, Omid-Zohoor '072 is shown to teach all the features of the claim with the exception of further includes forming a doped region below the termination of each isolation trench.

However, Poon further teaches forming a doped region (30) below the termination of each isolation trench (22) within the semiconductor substrate (12). (See Fig. 4).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to further form a doped region below the termination of each isolation trench within the semiconductor substrate of Omid-Zohoor as taught by Poon to prevent the field inversion.

With respect to claim 6, the upper surface for each isolation trench (376) of Omid-Zohoor '072 is formed by CMP. (See Fig. 3M, col. 4, ll. 47-62).

With respect to claim 7, Omid-Zohoor '072 teaches a method of forming a microelectronic structure substantially as claimed including:

forming an oxide layer (340) upon a semiconductor substrate (120);

forming a first dielectric layer (344) upon the oxide layer;

selectively removing the first dielectric layer (344) to exposed the oxide layer (340) at a plurality of areas;

forming a second dielectric layer (352) conformally over the oxide layer (340) and the first dielectric layer (344);

selectively removing the second dielectric layer (352) to form a plurality of spacers (356) from the second dielectric layer, wherein each spacer (356) is situated upon the oxide layer (340), is in contact with the first dielectric layer (344), and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches (360) extending below the oxide layer (340) into the semiconductor substrate (120), wherein each the isolation trench is adjacent to and below the pair of the spacers (356) and is situated at the corresponding area of the plurality of areas and wherein each isolation trench has an edge;

filling each the isolation trench (360) with a conformal layer (364), the conformal layer extending above the oxide layer (340) in contact with the corresponding pair of the spacers (356), wherein filling is performed by depositing the conformal layer and the depositing is carried out to the extent of filling each of the isolation trench (360) and extending over the spacers (356) and over the first dielectric layer (344) so as to define an upper surface contour of the conformal layer (364);

substantially simultaneously subjecting the entire upper surface contour of the conformal layer to a planarizing process and planarizing the conformal layer (364) to form therefrom an upper surface for each of the isolation trench (360) that is co-planar to the other upper surfaces, (see Fig. 3L-M), wherein:

the conformal layer (364) comprises a material that is electrically insulative and extends continuously between and within the plurality of isolation trenches (360);

the conformal layer (364) and the spacers (356) form the upper surface for each isolation trench, each upper surface being formed from the conformal layer (364) and the spacer (356) and being situated above the oxide layer (340); and

the first dielectric layer (344) is in contact with at least a pair of the spacers (356) and the oxide layer (340). (See Figs. 3A-M).

Thus, Omid-Zohoor '072 is shown to teach all the features of the claim with the exception of rounding the top edge of each of the isolation trenches.

However, Poon teaches that it is well known in the art to form a liner (28) upon the sidewall of each isolation trench (22) to remove damage caused by the trench-etch, the formation of the liner inherently rounding the top edge of the isolation trenches.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to form the liner upon the sidewall of each isolation trench of Omid-Zohoor '072 as taught by Poon to remove the damage caused by the trench-etch while rounding of the top edge reduces leakage current. These are well known in the art. See Wolf et al. of record.

With respect to claim 8, the method of Omid-Zohoor '072 further includes:

removing the oxide layer (340) upon a portion of the surface of semiconductor substrate (120); (Fig. 3O); and

forming a gate oxide layer (380) upon the portion of the surface of the semiconductor substrate. (See Fig. 3P).

With respect to claims 9 and 10, as best understood by the examiner, the method of Omid-Zohoor '072 further include removing the first dielectric layer (344) using an etch recipe that etches the first dielectric layer (344) faster than the conformal layer (364) and the spacers (356). (See Fig. 3N).

With respect to claim 11, the upper surface for each isolation trench (376) of Omid-Zohoor '072 is formed by:

chemical mechanical planarization, CMP, wherein the conformal layer (364), the spacers (356), and the first dielectric layer (344) form a planar first upper surface; (Fig. 3M); and

an etch that forms a second upper surface, the second upper surface being situated above the pad oxide layer (340). (Fig. 3N).

With respect to claims 12 and 13, as best understood by the examiner, the etch that forms a second upper surface uses an etch recipe that etches the first dielectric layer (344) faster than the conformal layer (364) and the spacers (356).

With respect to claim **14**, Omid-Zohoor '072 teaches a method of forming a microelectronic structure substantially as claimed including:

forming an oxide layer (340) upon a semiconductor substrate (120);

forming a silicon nitride layer (344) upon the oxide layer (340);

selectively removing the silicon nitride layer (344) to exposed the oxide layer (340) at a plurality of areas;

forming a first silicon dioxide layer (352) over the oxide layer (340) and the silicon nitride layer (344), wherein the forming of the first silicon dioxide layer (352) includes forming a first silicon dioxide layer (252) on and in contact with the exposed oxide layer (340) at the plurality of areas;

selectively removing the first silicon dioxide layer (352) to form a plurality of spacers (356) from the first silicon dioxide layer (352), wherein each spacer (356) is situated upon the oxide layer (340), is in contact with the silicon nitride layer (344), and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches (360) extending below the oxide layer (340) into and terminating within the semiconductor substrate (120), wherein each isolation trench (360) is adjacent to and below a pair of the spacers (356) and is situated at a corresponding area of the plurality of areas, and wherein each isolation trench has a top edge;

filling each isolation trench (360) with a conformal second silicon dioxide layer (364), the conformal second silicon dioxide layer within each isolation trench extending above the oxide layer (340) in contact with a corresponding pair of the spacers (356), wherein the filling is performed by depositing the conformal second silicon dioxide layer (364), and the depositing is carried out to the extent of filling each isolation trench (360) and extending over the spacers (356) and the silicon nitride layer (344) so as to define an upper surface contour of the second silicon dioxide layer (364); and

substantially simultaneously subjecting the entire upper surface contour of the conformal second silicon dioxide layer (364) to a planarizing process so as to remove the conformal second silicon dioxide layer (364) and the spacers (356) to form an upper surface for each isolation

trench that is co-planar to the other upper surfaces and being situated above the oxide layer (340), wherein the conformal second silicon dioxide layer (364) is an electrically insulative extends continuously between and within the plurality of isolation trenches. (See Figs. 3A-M).

Thus, Omid-Zohoor '072 is shown to teach all the features of the claim with the exception of forming a corresponding electrically active region below the termination of each isolation trench and forming a liner upon the sidewall of each isolation trench.

However, Poon teaches a method of forming a microelectronic structure including: forming a corresponding electrically active region (30) below the termination of each isolation trench (22) within the semiconductor substrate (12); and forming liner (28) upon the sidewall of each isolation trench, the liner being confined preferentially within each isolation trench and extending from the interface thereof with the oxide layer (14) to the termination of isolation trench within the semiconductor substrate (12). (See Figs. 3-4).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the corresponding electrically active region below the termination of each isolation trench and the liner upon the sidewall of each isolation trench of Omid-Zohoor '072 as taught by Poon to remove the damage caused by the trench-etch and to prevent field inversion. These are well known in the art. See Wolf et al..

With respect to claim 15, the liner (28) of Poon is a thermally grown oxide of the semiconductor substrate.

With respect to claim 16, the liner of Poon is also composed of silicon nitride (50). (See Fig. 12).

With respect to claim 17, the process of Omid-Zohoor '072 further includes:

removing the oxide layer (340) upon a portion of the surface of the semiconductor substrate (120); (Fig. 3O); and

forming a gate oxide layer (380) upon the portion of the surface of semiconductor substrate (120). (See Fig. 3P).

With respect to claim **18**, Omid-Zohoor '072 teaches a method of forming a microelectronic structure substantially as claimed including:

forming an oxide layer upon a semiconductor substrate (120);

forming polysilicon layer upon the oxide layer; (see col. 4, ll. 14-16);

forming a first dielectric layer (344) upon the polysilicon layer;

selectively removing the first dielectric layer (344) to exposed the oxide layer at a plurality of areas;

forming a second dielectric layer (352) conformally over the oxide layer, the polysilicon layer, and the first dielectric layer (344), wherein forming the second dielectric layer (352) includes forming the second dielectric layer (352) on and in contact with the exposed oxide layer at the plurality of areas;

selectively removing the second dielectric layer (352) to form a plurality of spacers (356) from the second dielectric layer, wherein each spacer is situated upon the oxide layer, is in

contact with both polysilicon layer and the first dielectric layer (344), and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches (360) extending below the oxide layer and from top edges into and terminating within the semiconductor substrate (120), wherein each isolation trench is adjacent to and below a pair of the spacers (356) and is situated at a corresponding area of the plurality of areas;

filling each isolation trench (360) with a conformal third layer (364), the conformal third layer extending above the oxide layer in contact with a corresponding pair of the spacers (356), wherein filling is performed by depositing the conformal third layer (364), and depositing is carried out to the extent of filling each isolation trench (360) and extending over the spacers (356) and over the first dielectric layer (344) so as to define an upper surface contour of the conformal third layer (364);

substantially simultaneously subjecting the entire upper surface contour of the conformal layer to a planarizing process and planarizing the conformal third layer (364) to form therefrom an upper surface for each isolation trench that is co-planar to the other upper surface;

wherein the conformal third layer (364) is an electrically insulative extends continuously between and within the plurality of isolation trenches; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers (356), the conformal third layer (364), and the plurality of isolation trench. (See Figs. 3A-M).

Thus, Omid-Zohoor '072 is shown to teach all the features of the claim with the exception of rounding the top edge of each of the isolation trenches and exposing the oxide layer.

However, Omid-Zohoor '104 teaches that it is well known in the art to form a liner (58a) upon the sidewall of each isolation trench to remove damage caused by the trench-etch, the formation of the liner inherently rounding the top edge of the isolation trenches. (See Fig. 3H).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the liner upon the sidewall of each isolation trench of Omid-Zohoor '072 as taught by Omid-Zohoor '104 to remove the damage caused by the trench-etch while rounding of the top edge reduces leakage current. These are well known in the art. See Wolf et al..

Regarding exposing the oxide layer, although Omid-Zohoor '072 does not explicitly disclose removing the polysilicon layer to expose the oxide layer.

However, Omid-Zohoor clearly teaches that a thin thermally-grown silicon oxide and a buffer polysilicon layer may be used for the pad oxide 340. (See col. 4, lines 14-16). Also, Omid-Zohoor clearly intended for the spacers (356) to be formed on the thermally-grown oxide layer (34). (See Figs. 3E-H).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to remove the first dielectric layer (344) and the polysilicon layer to expose the oxide layer as shown in Fig. 3E, without departing from the scope of Omid-Zohoor's invention, to form a T-shape isolation.

With respect to claim 19, the upper surface for each isolation trench (376) of Omid-Zohoor '072 is formed by CMP.

With respect to claim 20, in view of Poon, the process further comprises forming a doped region below the termination of each isolation trench within the semiconductor substrate. (See claim 5 above).

With respect to claim 21, as best understood by the examiner, the process of Omid-Zohoor '072, in view of Poon, further comprises: prior to filling each isolation trench with the conformal third layer, forming a liner (28) upon the sidewall of the isolation trench, the liner (28) being confined preferentially within each isolation trench and extending from an interface thereof with the oxide layer (14) to the termination of the isolation trench (22) within the semiconductor substrate, and wherein the conformal third layer (364) is composed of electrically insulative material.

With respect to claim 22, the liner (28) of Poon is a thermally grown oxide of the semiconductor substrate.

With respect to claim **24**, Omid-Zohoor '072 teaches a method of forming a microelectronic structure substantially as claimed including:

forming an oxide layer upon a semiconductor substrate (120);

forming polysilicon layer upon the oxide layer; (see col. 4, ll. 14-16);

forming a first dielectric layer (344) upon the polysilicon layer;

selectively removing the first dielectric layer (344) to exposed the oxide layer at a plurality of areas;

forming a second dielectric layer (352) conformally over the oxide layer, the polysilicon layer, and the first dielectric layer (344), wherein forming the second dielectric layer (352)

includes forming the second dielectric layer (352) on and in contact with the exposed oxide layer at the plurality of areas;

selectively removing the second dielectric layer (352) to form a plurality of spacers (356) from the second dielectric layer, wherein each spacer is situated upon the oxide layer, is in contact with both polysilicon layer and the first dielectric layer (344), and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches (360) extending below the oxide layer and from top edges into and terminating within the semiconductor substrate (120), wherein each isolation trench is adjacent to and below a pair of the spacers (356) and is situated at a corresponding area of the plurality of areas;

filling each isolation trench (360) with a conformal third layer (364), the conformal third layer extending above the oxide layer in contact with a corresponding pair of the spacers (356), wherein filling is performed by depositing the conformal third layer (364), and depositing is carried out to the extent of filling each isolation trench (360) and extending over the spacers (356) and over the first dielectric layer (344) so as to define an upper surface contour of the conformal third layer (364);

substantially simultaneously subjecting the entire upper surface contour of the conformal layer to a planarizing process and planarizing the conformal third layer (364) to form therefrom an upper surface for each isolation trench that is co-planar to the other upper surface;

wherein the conformal third layer (364) is an electrically insulative extends continuously between and within the plurality of isolation trenches;

wherein the upper surface of each isolation trench is formed from the conformal third layer (364), the spacers (356), and the first dielectric layer (344); and

wherein the microelectronic structure is defined at least in part by the plurality of spacers (356), the conformal third layer (364), and the plurality of isolation trench. (See Figs. 3A-M).

Thus, Omid-Zohoor '072 is shown to teach all the features of the claim with the exception of rounding the top edge of each of the isolation trenches and exposing the oxide layer.

However, Omid-Zohoor '104 teaches that it is well known in the art to form a liner (58a) upon the sidewall of each isolation trench to remove damage caused by the trench-etch, the formation of the liner inherently rounding the top edge of the isolation trenches. (See Fig. 3H).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the liner upon the sidewall of each isolation trench of Omid-Zohoor '072 as taught by Omid-Zohoor '104 to remove the damage caused by the trench-etch while rounding of the top edge reduces leakage current. These are well known in the art. See Wolf et al..

Regarding exposing the oxide layer, although Omid-Zohoor '072 does not explicitly disclose removing the polysilicon layer to expose the oxide layer.

However, Omid-Zohoor clearly teaches that a thin thermally-grown silicon oxide and a buffer polysilicon layer may be used for the pad oxide 340. (See col. 4, lines 14-16). Also, Omid-Zohoor clearly intended for the spacers (356) to be formed on the thermally-grown oxide layer (34). (See Figs. 3E-H).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to remove the first dielectric layer (344) and the polysilicon layer to expose the oxide layer as shown in Fig. 3E, without departing from the scope of Omid-Zohoor's invention, to form a T-shape isolation.

With respect to claim **25**, as best understood by examiner, Omid-Zohoor '072 teaches a method of forming a microelectronic structure substantially as claimed including:

forming an oxide layer upon a semiconductor substrate (120);

forming polysilicon layer upon the oxide layer; (see col. 4, ll. 14-16);

forming a first dielectric layer (344) upon the polysilicon layer;

selectively removing the first dielectric layer (344) to exposed the oxide layer at a plurality of areas;

forming a second dielectric layer (352) conformally over the oxide layer, the polysilicon layer, and the first dielectric layer (344), wherein the forming a second dielectric layer (352) includes forming a second dielectric layer (352) on and in contact with the exposed oxide layer at the plurality of areas;

selectively removing the second dielectric layer (352) to form a plurality of spacers (356) from the second dielectric layer, wherein each spacer is situated upon the oxide layer, is in contact with both polysilicon layer and the first dielectric layer (344), and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches (360) extending below the oxide layer and from top edges into and terminating within the semiconductor substrate (120), wherein each isolation

trench of the plurality of isolation trenches is adjacent to and below a pair of the spacers (356) and is situated at a corresponding area of the plurality of areas;

filling each isolation trench (360) with a conformal third layer (364), the conformal third layer extending above the oxide layer in contact with a corresponding pair of the spacers (356), wherein the filling is performed by depositing the conformal third layer (364), and the depositing is carried out to the extend of filling each isolation trench (360) and extending over the spacers (356) and over the first dielectric layer (344) so as to define an upper surface contour of the conformal third layer (364);

substantially simultaneously subjecting the entire upper surface contour of the conformal layer to a planarizing process and planarizing the conformal third layer (364) to form therefrom an upper surface for each isolation trench that is co-planar to the other upper surface;

exposing the oxide layer (340) upon a portion of the surface of the semiconductor substrate (120);

forming a gate oxide layer (380) upon the portion of the surface of the semiconductor substrate (120);

forming in between the isolation trench, and confined in the space therebetween, a layer composed of polysilicon upon the oxide layer in contact with the pair of the spacers (356); and

selectively removing the conformal third layer (364), the spacers (356) and the layer composed of polysilicon to form a portion of at least one of the upper surfaces;

wherein the conformal third layer comprises a material that is electrically insulative extends continuously between and within the plurality of isolation trenches. (See Fig. 3A-M).

With respect to rounding the top edge of each isolation trenches and removing the polysilicon layer to expose the oxide layer, the similar reason as that of claims 18 and 24 is also applied here.

With respect to claim **26**, as best understood by examiner, Omid-Zohoor '072 teaches a method of forming a microelectronic structure substantially as claimed including:

forming an oxide layer upon a semiconductor substrate (120);

forming polysilicon layer upon the oxide layer; (see col. 4, ll. 14-16);

forming a first dielectric layer (344) upon the polysilicon layer;

selectively removing the first dielectric layer (344) to exposed the oxide layer at a plurality of areas;

forming a second dielectric layer (352) conformally over the oxide layer, the polysilicon layer, and the first dielectric layer (344), wherein the forming a second dielectric layer (352) includes forming a second dielectric layer (352) on and in contact with the exposed oxide layer at the plurality of areas;

selectively removing the second dielectric layer (352) to form a plurality of spacers (356) from the second dielectric layer, wherein each spacer of the plurality of spacers is upon the oxide layer, is in contact with both polysilicon layer and the first dielectric layer (344), and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches (360) extending below the oxide layer and from top edges into and terminating within the semiconductor substrate (120), wherein each isolation

trench of the plurality of isolation trenches is adjacent to and below a pair of the spacers (356) and is situated at a corresponding area of the plurality of areas;

filling each isolation trench (360) with a conformal third layer (364), the conformal third layer extending above the oxide layer in contact with a corresponding pair of the spacers (356), wherein the filling is performed by depositing the conformal third layer (364), and the depositing is carried out to the extend of filling each isolation trench (360) and extending over the spacers (356) and over the first dielectric layer (344) so as to define an upper surface contour of the conformal layer (364);

substantially simultaneously subjecting the entire upper surface contour of the conformal third layer to a planarizing process comprising an etch recipes that etches the conformal third layer (364) and the spacers (356) faster than first dielectric layer (344) by a ratio in a range from about 1:1 to about 2:1 and planarizing the conformal third layer (364) to form therefrom an upper surface for each isolation trench that is co-planar to the other upper surface;

wherein the conformal third layer (364) comprises a material that is electrically insulative extends continuously between and within the plurality of isolation trenches; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers (356), the conformal third layer (364) and the plurality of isolation trenches. (See Figs. 3A-M).

With respect to rounding the top edge of each isolation trenches and removing the polysilicon layer to expose the oxide layer, the similar reason as that of claims 18 and 24 is also applied here.

Regarding the etch ratio in the range from about 1:1 to about 2:1, since the etch of Omid-Zohoor result in a planar surface, Fig. 3M, the etch ratio is at least 1:1.

With respect to claim **31**, as best understood by examiner, Omid-Zohoor '072 teaches a method of forming a microelectronic structure substantially as claimed including:

forming a pad oxide layer upon a semiconductor substrate (120);

forming polysilicon layer upon the oxide layer; (see col. 4, ll. 14-16);

forming a silicon nitride layer (344) upon the polysilicon layer;

selectively removing the silicon nitride layer (344) to exposed the pad oxide layer at a plurality of areas;

forming a first silicon dioxide layer (352) conformally over the pad oxide layer and over the silicon nitride layer (344), wherein the forming of the first silicon dioxide layer (352) includes forming the first silicon dioxide layer (352) on and in contact with the exposed oxide layer at the plurality of areas;

selectively removing the first silicon dioxide layer (352) to form a plurality of spacers (356) from the first silicon dioxide layer, wherein each spacer (356) of the plurality of spacers is situated upon the pad oxide layer, is in contact with the silicon nitride layer (344) and the polysilicon layer, and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches (360) extending below the oxide layer and from top edges into and terminating within the semiconductor substrate (120), wherein each isolation trench of the plurality of isolation trenches is adjacent to and below a pair of the spacers (356) and is situated at a corresponding area of the plurality of areas;

filling each isolation trench (360) with a conformal second layer (364), the conformal second layer extending above the pad oxide layer in contact with a corresponding pair of the spacers (356), wherein the filling is performed by depositing the conformal second layer (364), and the depositing is carried out to the extend of filling each isolation trench (360) and extending over the spacers (356) and over the silicon nitride layer (344) so as to define an upper surface contour of the conformal second layer (364); and

substantially simultaneously subjecting the entire upper surface contour of the conformal second layer to a planarizing process and planarizing the conformal second layer (364) and each of the spacers (356) to form therefrom an upper surface for each isolation trench that is co-planar to the other upper surface and is situated above the pad oxide layer (340);

wherein the conformal second layer (364) comprises a material that is electrically insulative extends continuously between and within the plurality of isolation trenches. (See Figs. 3A-M).

Thus, Omid-Zohoor '072 is shown to teach all the features of the claim with the exception of forming a corresponding doped region below the termination of each isolation trench, forming a liner upon the sidewall of each isolation trench and exposing the oxide layer.

However, Poon teaches a method of forming a microelectronic structure including: forming a corresponding doped region (30) below the termination of each isolation trench (22) within the semiconductor substrate (12); and forming liner (28) upon the sidewall of each isolation trench, the formation of the liner (28) inherently results in rounding of the top edge of the isolation trench. (See Figs. 3-4).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the corresponding electrically active region below the termination of each isolation trench and the liner upon the sidewall of each isolation trench of Omid-Zohoor '072 as taught by Poon to remove the damage caused by the trench-etch and to prevent field inversion. These are well known in the art. See Wolf et al..

With respect to removing the silicon nitride layer and the polysilicon layer to expose the oxide layer, the similar reason as that of claims 18 and 24 is also applied here.

With respect to claim 32, the liner (28) of Poon is a thermally grown oxide of the semiconductor substrate and the conformal second layer (364) of Omid-Zohoor is composed of an electrically insulative material.

With respect to claim 33, in view of Poon, the liner is also composed of silicon nitride (50) and the conformal second layer of Omid-Zohoor or Poon is composed of an electrically insulative material.

With respect to claim 34, as best understood by the examiner, the method of Omid-Zohoor further comprises: (also see claim 25):

exposing the oxide layer (340) upon a portion of the surface of the semiconductor substrate (120); (see Fig. 3N);

forming a gate oxide layer (380) upon the portion of the surface of the semiconductor substrate (120); (see Fig. 3P);

forming between the plurality of isolation trenches (360), and confined in the space therebetween, a layer composed of polysilicon upon the oxide layer in contact with the pair of the spacers (356); and

selectively removing the layer composed of polysilicon to form a portion of at least one of the upper surfaces. (See Fig. 3N).

6. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Omid-Zohoor '072 and Poon as applied to claim 26 above, and further in view of Miyashita et al. (U.S. Patent No. 6,069,083) of record.

Omid-Zohoor teaches planarizing the conformal third layer (364) by an etch using an etch recipe that etches the conformal third layer (364) and the spacers (356) faster than the first dielectric layer (344).

Thus, Omid-Zohoor is shown to teach all the features of the claim with the exception of explicitly utilizing an ratio in the range from about 1.3:1 to about 1.7:1.

However, Miyashita teaches planarizing the conformal layer (6) by an etch using an etch recipe that etches the conformal layer (6) faster than the first dielectric layer (2) by a ratio in a range from about 1 (1:1) to about 3 (3:1), which encompasses the claimed range.

Note that the specification contains no disclosure of either the *critical nature of the claimed etch ratios* of any unexpected results arising therefrom. Where patentability is aid to based upon particular chosen dimension or upon another variable recited in a claim, the Applicant must show that the chosen dimension are critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to planarize the conformal third layer of Omid-Zohoor '072 utilizing an etch ratio as taught by Miyashita to form the upper surface of the microelectronic structure.

7. Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Omid-Zohoor '072.

With respect to claim **35**, as best understood by the examiner, Omid-Zohoor teaches a method of forming a microelectronic structure substantially similar as claimed including:

providing a semiconductor substrate (120) having a top surface with an oxide layer thereon;

forming a polysilicon layer upon the oxide layer; (col. 4, ll.14-16);

forming a first layer (344) upon the polysilicon layer;

selectively removing the first layer (344) and the polysilicon layer to expose the oxide layer at a plurality areas;

forming a plurality of isolation trenches (360) through the exposed oxide layer at the plurality of areas, wherein an electrically insulative material (364) extends continuously between and within the plurality of isolation trenches, each isolation trench (360):

having a spacer (356) composed of a dielectric material upon the oxide layer in contact with the first layer (344) and the polysilicon layer;

extending from an opening thereto at the top surface of the semiconductor substrate and below the oxide layer into and terminating within the semiconductor substrate adjacent to and below the spacer;

having a second layer (364) filling the isolation trench (360) and extending above the oxide layer in contact with the spacer (356), wherein the filling is performed by depositing the second layer, and depositing is carried out to the extent of filling each isolation trench (360) and extending over the spacers (356) and over the first layer (344)so as to define an upper surface contour of the second layer; and

having a planar upper surface formed from the second layer (364) and the spacer (356) and being situated above the oxide layer, wherein the planar upper surface is formed by substantially simultaneously subjecting the entire upper surface contour of the conformal layer to planarizing process; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers (356), the second layer (364), and the plurality of isolation trenches (360). (See Figs. 3A-M).

Although Omid-Zohoor '072 does not explicitly disclose removing the polysilicon layer to expose the oxide layer.

However, Omid-Zohoor clearly teaches that a thin thermally-grown silicon oxide and a buffer polysilicon layer may be used for the pad oxide 340. (See col. 4, lines 14-16). Also, Omid-Zohoor clearly intended for the spacers (356) to be formed on the thermally-grown oxide layer (34). (See Figs. 3E-H).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to remove the first layer and the polysilicon layer of Omid-Zohoor '072 to expose the oxide layer as shown in Fig. 3E, without departing from the scope of Omid-Zohoor's invention, to form a T-shape isolation.

8. Claims 36-37 and 39-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Omid-Zohoor '072 as applied to claims 35 and 38 above, and further in view of Wolf *Silicon Processing for the VLSI Era*, Vol. 2, pp. 54-55, all of record.

With respect to claims 36 and 39, Omid-Zohoor '072 is shown to teach all the features of the claim with the exception of further includes forming a doped region below the termination of each isolation trench.

However, Wolf, from Fig. 2-37, page 54, teaches forming of trench isolation including:

doping the semiconductor substrate with a dopant having a first conductivity type (n);

doping the semiconductor substrate below each isolation trench with a dopant having a second conductivity type (p) opposite the first conductivity type to form a doped trench bottom that is below and in contact with a respective one isolation trench.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to further form a doped region in the substrate below each isolation trench of Omid-Zohoor as taught by Wolf to prevent the field inversion.

With respect to claims 37 and 40, the doped trench bottom of Wolf has a width, each isolation trench has a width, and the width of each doped trench bottom is greater than that of the respective isolation trench. (See Fig. 2-37).

9. Claims **42** and **43** are rejected under 35 U.S.C. 103(a) as being unpatentable over Omid-Zohoor '072 in view of Wolf *Silicon Processing for the VLSI Era*, Vol. 2, pp. 54-55.

With respect to claim **42**, Omid-Zohoor '072 teaches a method for forming a microelectronic structure substantially similar as claimed including:

providing a semiconductor substrate (120) having a top surface with an oxide layer thereon;

forming a polysilicon layer upon the oxide layer; (col. 4, ll. 14-16);

forming a first layer (344) upon the polysilicon layer;

forming a first isolation structure including:

a first spacer (356) composed of a dielectric material upon the oxide layer in contact with the first layer (344) and the polysilicon layer;

a first isolation trench (360) extending from an opening thereto at the top edges at the top surface of the semiconductor substrate (120) and below the oxide layer (340) into and terminating within the semiconductor substrate adjacent to and below the first spacer (356), wherein the first spacer is situated on a side of the first isolation trench, and wherein the first isolation trench has a top edge;

a second spacer (356) composed of a dielectric material upon the oxide layer in contact with the first layer, the second spacer being situated on a side of the first isolation trench opposite the side of the first spacer;

forming a second isolation structure including:

a first spacer (356) composed of a dielectric material upon the oxide layer in contact with the first layer (344) and the polysilicon layer;

a first isolation trench (360) extending from an opening thereto at the top edges at the top surface of the semiconductor substrate (120) and below the oxide

layer (340) into and terminating within the semiconductor substrate adjacent to and below the first spacer (356), wherein the first spacer is situated on a side of the first isolation trench, and wherein the first isolation trench has a top edge;

a second spacer (356) composed of a dielectric material upon the oxide layer in contact with the first layer, the second spacer of the second isolation structure being situated on a side of the first isolation trench opposite the side of the first spacer of the second isolation structure;

forming an active area located within the semiconductor substrate between the first and second isolation structures;

forming a conformal second layer (364), composed of an electrically insulative material, filling the first and second isolation trenches and extending continuously therebetween and above the oxide layer in contact with the first and second spacers (356) of the respective first and second isolation structures (360), wherein filling is performed by depositing the conformal second layer (364), and the depositing is carried out to the extent of filling each isolation trenches and extending over the spaces (356) and the first layer (344) so as to define an upper surface contour of the conformal second layer (364);

substantially simultaneously subjecting the entire upper surface contour of the conformal second layer to planarizing process and

forming a planar upper surface from the conformal second layer (364) and the first and second spacers (356) of the respective first and second isolation structures and being situated above the oxide layer; and

wherein the microelectronic structure is defined at least in part by the active area, the conformal second layer (364), and the first and second isolation trenches. (See Figs. 3A-M).

Thus, Omid-Zohoor '072 is shown to teach all the features of the claim with the exception of explicitly disclosing the removal of polysilicon layer exposing the oxide layer, and rounding the top edges of the isolation trench.

However, although Omid-Zohoor '072 does not explicitly disclose removing the polysilicon layer to expose the oxide layer, but Omid-Zohoor clearly teaches that a thin thermally-grown silicon oxide and a buffer polysilicon layer may be used for the pad oxide 340. (See col. 4, lines 14-16). Also, Omid-Zohoor clearly intended for the spacers (356) to be formed on the thermally-grown oxide layer (34). (See Figs. 3E-H).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to remove the first layer and the polysilicon layer of Omid-Zohoor '072 to expose the oxide layer as shown in Fig. 3E, without departing from the scope of Omid-Zohoor's invention, to form a T-shape isolation.

Further, with respect to rounding the top edge of the isolation trench, Wolf, from Fig. 2-38, and page 55, teaches that it is well known in the art to form a rounded top edge of the isolation trench by forming a thermal liner.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the isolation trench of Omid-Zohoor '072 having top edge that is rounded as taught by Wolf to remove damage caused by the trench etch while rounding the top edge in the process.

With respect to claim **43**, Omid-Zohoor teaches a method for forming a microelectronic structure substantially similar as claimed including:

providing a semiconductor substrate (120) having a top surface with an oxide layer (340) thereon;

forming a first layer (344) upon the oxide layer;

forming a first isolation structure including:

a first spacer (356) composed of a dielectric material upon the oxide layer (340) in contact with the first layer (344);

a first isolation trench (360) extending from an opening thereto at the top surface of the semiconductor substrate (120) and below the oxide layer (340) into and terminating within the semiconductor substrate adjacent to and below the first spacer (356), wherein the first spacer is situated on a side of the first isolation trench, and wherein the first isolation trench has a top edge; and

a second spacer (356) composed of a dielectric material upon the oxide layer (340) in contact with the first layer, the second spacer being situated on a side of the first isolation trench opposite the side of the first spacer;

forming a second isolation structure including:

a first spacer (356) composed of a dielectric material upon the oxide layer in contact with the first layer (344);

a first isolation trench (360) extending below the oxide layer (340) into and terminating within the semiconductor substrate adjacent to and below the first spacer

(356), wherein the first spacer of the second isolation structure is situated on a side of the first isolation trench, and wherein the first isolation trench has a top edge; and

a second spacer (356) composed of a dielectric material upon the oxide layer (340) in contact with the first layer, the second spacer of the second isolation structure being situated on a side of the first isolation trench opposite the side of the first spacer of the second isolation structure;

forming an active area located within the semiconductor substrate between the first and second isolation structures;

forming a conformal second layer (364), composed of an electrically insulative material, conformally filling the first and second isolation trenches and extending continuously therebetween and above the oxide layer (340) in contact with the first and second spacers (356) of the respective first and second isolation structures, wherein filling is performed by depositing the conformal second layer (364), and the depositing is carried out to the extent of filling each isolation trench and extending over the spaces (356) and the first layer (344) so as to define an upper surface contour of the conformal second layer (364); and

substantially simultaneously subjecting the entire upper surface contour of the conformal layer to planarizing process and planarizing the conformal second layer (364) and the first and second spacers (356) of the respective first and second isolation structures to form a planar upper surface from the conformal second layer (364) and the first and second spacers (356) of respective first and second isolation structures, and being situated above the oxide layer, wherein the microelectronic structure is defined at least in part by the active area, the conformal second layer (364), and the first and second isolation trenches. (See Figs. 3A-M).

With respect to the rounding of the top edges of the isolation trench, a similar reason as that of claim 42 is also applied here.

Response to Arguments

10. Applicant's arguments filed December 11, 2006 have been fully considered but they are not persuasive.

Claim Rejection Under 35 U.S.C. 112, first and second paragraph:

Claims 9, 10, 12 and 13 claiming the removal of the first dielectric layer. However, the claimed ratio belongs to the planarization of the conformal layer, not the first dielectric layer. See specification page 14. This is a classical mix-and-match of the **wrong things**. Since the specification discloses two types of etch, one with a ratio ranges and one without any ratio, thus, one ratio can not be used for the other. Therefore, claiming one type of etch, "first dielectric layer" with the ratio of the other etch, "conformal layer", constitutes new matters, first paragraph, and contradictory, second paragraph.

Claim 21, Applicant refers to page 12, for support. This is an alternative to form the liner oxide, CVD instead of thermal oxide. As discussed many times before, a limitation of claim 18 includes: "**rounding the top edges** of the isolation trenches". By claiming "rounding of the edges" the limitation **implicitly includes thermal liner**. The specification does not support two liners, one formed by "rounding the top edges" and one by CVD.

Furthermore, according to claim 22, the liner is thermally grown oxide of the semiconductor substrate. This also contradicting the applicant argument.

Therefore, claim 21 clearly a new matters.

The rejections are therefore, maintained.

Rejection under 35 U.S.C. 103(a)

The new limitation "substantially simultaneously subject the entire upper surface contour of the conformal layer to a planarizing process" fails to overcome the teaching of Omid-Zohoor '072, both wet etch and CMP of Omid-Zohoor is a planarizing process, e.g., removing conformal layer to planarize the top surface of the isolation trench.

The amended claims 35 and 38 have resulted in new ground of rejections.

Since Omid-Zohoor clearly teaches the new limitation, the combination of Omid-Zohoor and the secondary references clearly rendered the claims obvious.

The rejections of all claims are therefore, maintained.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (571) 272-1710. The examiner can normally be reached on 8:00AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

ANH D. MAI
PRIMARY EXAMINER